CLAIMS

1. An analog to digital converter ("ADC"), comprising:

a band gap reference (BGR) circuit whose output is internally coupled to an analog input of the ADC.

2. The ADC of Claim 1, further comprising:

a positive analog supply voltage (AVDD) and a positive analog reference voltage (REFP) operationally coupled to a same voltage supply; wherein a BGR value is used by a CPU as a calibration constant for determining an AVDD value.

3. The ADC of Claim 1, wherein the ADC can measure the AVDD without using a divider.

4. The ADC of Claim 1, wherein the measured BGR value is inversely proportional to the AVDD value.

5. A system using a CPU, comprising:

an analog to digital converter ("ADC"), wherein the ADC includes:

a band gap reference (BGR) circuit output internally coupled to an analog input to the ADC.

6. The system of Claim 5, further comprising:

a positive analog supply voltage (AVDD) and a positive analog reference voltage (REFP) operationally

coupled to same voltage supply; wherein a BGR value is used by the CPU as a calibration constant for determining an AVDD value.

7. The system of Claim 5, wherein the ADC can measure the AVDD without using a divider.

8. The system of Claim 5, wherein the measured BGR value is inversely proportional to the AVDD value.

9. An application specific integrated circuit ("ASIC"), comprising:

an analog to digital converter ("ADC"), comprising:

a band gap reference (BGR) circuit whose output is internally coupled to an analog input of the ADC.

10. The ASIC of Claim 9, further comprising:

a positive analog supply voltage (AVDD) and a positive analog reference voltage (REFP) operationally coupled to same voltage supply; wherein a BGR value is used by a CPU as a calibration constant for determining an AVDD value.

11. The ASIC of Claim 9, wherein the ADC can measure the AVDD without using a divider.

12. The system of Claim 9, wherein the measured BGR value is inversely proportional to the AVDD value.